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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/908,948	07/19/2001	Kenneth P. Parker	10001121-1	1925

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/908,948	PARKER, KENNETH P.
	Examiner	**Art Unit**
	Esaw T Abraham	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Final rejection

Response to the applicant's amendments

**********The objection of record to the drawings is withdrawn in response to applicant's amendment.

**********The 112, 2nd paragraph rejection of record is withdrawn in response to applicant's amendment.

Response to the applicant's argument

Applicants' argument/amendments with respect to amended claims 1, 9, 12, 14 and original claims 2-8, 11, 11, 13, 15-23 filed on 06/11/04 have been fully considered but are not persuasive. The examiner would like to point out that this action is made final (MPEP 706.07a).

Response to remark pages 12-15, the applicant argues that the prior art of record, Wagner et al. do not teach or discuss "transistors becoming hot or current surging" and instead Wagner teach race mitigation technique and further the applicant argues or fails to see how Wagner's delay elements would minimize current surges. However, the examiner disagrees because Wagner does teach scan shift race conditions are minimized by providing a weak scan output signal driver and inserting delay elements within a cell for scan flip-flop in the scan signal path (see abstract). Therefore, there is no difference between the applicant's minimizing a sudden current rise or surge (which the goal is to minimize a current error) and the minimization of scan shift race conditions in the prior art since the both the applicant's invention and Wagner's system minimizes current errors (current rises or races).

The applicant further argues (in claims 2-5) that the prior art do not teach or disclose that a number of gating signals disable current flow through the plurality of interconnected circuit elements.

However, the examiner disagrees and asserts that Wagner does teach race conditions during scan shift operations by decreasing (minimizing) its current drive capability of the inverter (61) whereby the inverter (61) loaded by another inverter (63) made a weak signal drive by decreasing its current drive wherein the process for the current drive capability decrease, affects the CMOS (transistor) (see col. 6, lines 16-45). Therefore, in light of the above, the final rejection holds strong in view of the recited references.

Furthermore, the applicant argues (in claims 6 and 7) that the prior arts do not teach or disclose first and second scan chains.

However, the examiner disagrees and asserts that the argument is not convincing because Wagner in figure 1 teach scan flip-flops 15A-G are formed into a serial scan chain, i.e., a serial shift register, by connecting the Q data output of one scan flip-flop to the S.sub.IN port of another scan flip-flop. Therefore, the argument is again acknowledged but is not convincing.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims **1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wagner et al. (U.S. PN: 6,389,566).

As per claims **1, 9, 12, 14, and 18,** Wagner et al. in figure 1 teach or disclose a digital logic circuit of a combinational circuit (11) has at least four outputs (17A-D), each of which is passed to the ports of the scan flip-flops (15A-D), are formed into a serial scan chain, i.e., a serial shift register, by connecting the Q data output of one scan flip-flop to the port of another scan flip-flop (see col. 1, last paragraph). Wagner et al. teach a scan flip-flop and methodology which reduces the possibility, among other items, of race problems during scan shift operations to control over circuit design elements (see col. 3, lines 39-43). Wagner et al. **do not explicitly** teach a current surge minimization circuit which is interconnected to the interconnected circuits. **However,** Wagner et al. teach a scan shift race conditions are minimized by providing a weak scan output signal driver and inserting delay elements within a cell for a scan flip-flop in the scan signal path (abstract, col. 3, lines 39-58) and further Wagner et al. teach a preceding equation for avoiding race conditions during scan shift operations (see col. 6, lines 15-30) including applying the functionality of CMOS device (In CMOS technology, both kinds of transistors (N-type transistors) or (P-type transistors) are used in a complementary way to form a current gate that

forms an effective means of electrical control and as the current direction changes more rapidly, however, the transistors become hot. This characteristic tends to limit the speed at which microprocessors can operate) for minimizing the race (surge) current (see col. 6, lines 31-45) which Wagner's system is basically teaching the same system and method as the applicant's claim to minimize current. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to minimize race or surge of currents. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to improve the efficiency of the test process and stabilizes the production lines.

As per claims **2, 3, 5, 10, 17, 19 and 20,** Wagner et al. teach all the subject matter claimed in claims 1 and 9, 14, 18 including Wagner teach race conditions during scan shift operations avoided by increasing the signal transition time of a flip-flop during a shift operation and by decreasing the current drive capability of the inverter (61) and further an inverter (63) presents load to the inverter (61) made a weak signal driver by decreasing its current drive capability and the current drive capability of the CMOS (transistors) device is proportional to the carrier mobility of the device (see col. 6, lines 16-45). Further, Wagner et al. teach that the scan-out signal driver is a weak current source and is therefore a weak signal driver and a circuit element, which may be a buffer, an inverter, or other simple logic gates, is inserted in the signal path prior to the scan-out signal driver to introduce delay in the scan-out signal path (see col. 3, lines 54-67).

As per claim **4,** Wagner et al. teach all the subject matter claimed in claims 1 and 3 including Wagner teach scan shift race conditions are minimized by providing a weak scan

output signal driver (signal generator) and inserting delay elements within a cell for a scan flip-flop in the scan signal path (see abstract).

As per claim **6,** Wagner et al. teach all the subject matter claimed in claims 1 including Wagner et al. in figure 1 teach or disclose digital logic circuit of a combinational circuit (11) has at least four outputs (17A-D), each of which is passed to the ports of the scan flip-flops (15A-D), are formed into a serial scan chain, i.e., a serial shift register, by connecting the Q data output of one scan flip-flop to the port of another scan flip-flop (see col. 1, last paragraph).

As per claims **7 and 8,** Wagner et al. teach all the subject matter claimed in claims 1 and 3 including Wagner teach scan shift race conditions are minimized by providing a weak scan output signal driver (signal generator) and inserting delay elements within a cell for a scan flip-flop in the scan signal path (see abstract).

As per claim **11,** Wagner et al. teach all the subject matter claimed in claim 9. Wagner et al. **do not explicitly** teach phasing operation. **Nevertheless,** as would have been well known to one ordinary skill in the art at the time the invention was made, performing a phase operation is required in most of scan testing systems since the operation commonly deals with different shifting signals (test data) between scan chains. **Accordingly,** it would have been obvious to one ordinary skill in the art to perform phase operations between the scan chains in order to distinguish the leading phase from the lagging phase.

As per claims **12 and 13,** Wagner et al. teach all the subject matter claimed in claims 1, 9 and 14 including Wagner teach a design circuit operation by using a high level language description (software) such as a hardware description language (HDL) provided to a compiler which creates a net list containing a specific logic components of the circuit and the connections

between the components that comprise the circuit wherein the compiler utilizes the net list to map specific cells from a cell library to each of the components or specify, actual circuit elements and furthermore placement of the scan flip-flops of figures 2 and 3, and variations thereof, in cells in the cell libraries allows a circuit designer to select appropriate scan flip-flops during the design phase, and allows the circuit designer to do so with the knowledge that a later formation of scan chains will not affect normal circuit operation. Thus, a synthesis post-process, in which scan candidate flip-flops are identified and replaced with scan flip-flops eliminated from the design process. Additionally, this one-pass scan synthesis process allows a circuit designer to see the timing, power size, and other impacts of scan flip-flops immediately during the design process (see col. 8, lines 16-38 and figure 7). Further, Wagner teach a method using a computer for designing a digital electronic circuit including scan flip-flops forming a scan chain based on a high level language description describing the functions of the digital electronic circuit comprising: generating a list including logic components and interconnections between the logic components from the high level language description (see claim 24).

As per claims **15 and 16,** Wagner et al. teach all the subject matter claimed in claim 14 including Wagner et al. teach mapping the flip-flop components to at least one scan flip-flop cell, the scan flip-flop cell specifying a flip-flop element having at least two inputs, a data input and a scan input, and at least two outputs, a data output and a scan output, with the data output driven by a data output signal driver and the scan output driven by a scan output signal driver, the scan output signal driver being a weak signal driver, the scan output signal driver receiving a signal from the data output signal driver, and the scan output signal driver presenting a substantially known load to the data output signal driver; and forming a representation of a

scan chain by linking a data output of a first of the plurality of scan flip-flop cells to a scan input of a second of the

Plurality of scans flip-flop cells (see claim 24 and col. 4, lines 13-28).

5. Claims **21-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. PN: 5,831,992).

As per claims **21-23,** Wu teach in figure 1 disclosed functional elements including pattern generator (12), which is capable of generating a plurality of pseudo-random test vectors whereby the functional elements (Scan chain 1 to Scan chain m) represent the circuit components within the circuit under test (CUT) for which fault diagnosis is required (see col. 4, lines 43-53). Wu further teach that all the scan chains are tested at the same time, and the test responses from all the scan chains are analyzed in parallel and when the scan chain fails an approach is to treat the multiple scan chains as multiple single scan chains, i.e., diagnose one chain at a time or in other words, the entire test set is applied to all the scan chains, but the test response from only a single chain is analyzed by gating the scan-out data (see in figure 2) and the controller (see element 18) is used to select the test responses (see col. 6, lines 45-59). Wu **does not explicitly** teach that the scan chains are out-of-phase. **However,** shifting test data through two scan chains out-of-phase is known in the art or common practice for most of scan testing systems because in-phase and out-of-phase have to do with the electrical cycle and when two signals are "in phase", they are oscillating "harmoniously" (or they are both negative or positive at the same time), and their combined output is increased while the two signals are "out-of-phase", they are oscillating "dies-harmoniously" (or one signal is negative when the

other is positive), and their combined output is obviously reduced. **Therefore,** it would have been obvious at the time the invention was made to one of ordinary skill in the art to design different time cycles for each of the scan chains **since** the method is conventional and well known.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,664,798 De Jong et al.

US PN: 4,307,342 Peterson

US PN: 4,075,549 Woodward

US PN: 5,864,457 Kates et al.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571)272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Esaw Abraham

Art unit: 2133

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